Amendments to the claims:

The claims in this listing will replace all prior claims in the application.

Listing of Claims:

1. (Currently Amended) A single transistor random access memory cell, comprising:

a transfer gate; ~~and~~

a storage capacitor with a storage node having an MOS native device with a near zero threshold voltage to form an inversion layer;

a shallow trench isolation, STI, insulator having a reduced step height below that of an overdoped OD sidewall of a substrate insulator; and

a capacitor plate covering the STI insulator and the overdoped OD sidewall.

2. (Original) The cell as in claim 1, further comprising:

an inversion region beneath the transfer gate, which is formed by diffusion of the inversion layer.

3. (Cancelled).

4. (Original) The cell as in claim 1, wherein

the transfer gate and a capacitor plate being closer together than a minimum line width of a single photomask.

5. (Original) The cell as in claim 4, further comprising:

a dielectric spacer between the transfer gate and the capacitor plate.

6. (Cancelled)

7. (Original) The cell as in claim 6, further comprising:

an inversion region beneath the transfer gate, which is formed by diffusion of the inversion layer.

8. (Original) The cell as in claim 6, wherein

the transfer gate has another MOS native device forming an inversion region at a near zero threshold voltage.

9. (Original) The cell as in claim 6, wherein

the transfer gate and a capacitor plate being closer together than a minimum line width of a single photomask.

10. (Original) The cell as in claim 6, further comprising:

a dielectric spacer between the transfer gate and the capacitor plate.

11. (Original) The cell as in claim 1, further comprising:

a shallow trench isolation, STI, insulator having a reduced step height below that of an OD sidewall of a substrate insulator;

the transfer gate and the capacitor being in an active area of the substrate;

an external MOS native device external to the active area, the external MOS native device forming an inversion layer at near zero threshold voltage; and

a capacitor plate covering the STI insulator and the external MOS native device.

12. (Original) The cell as in claim 11, further comprising:

an inversion region beneath the transfer gate, which is formed by diffusion of the inversion layer.

13. (Original) The cell as in claim 11, further comprising:

the transfer gate having an MOS native device forming an inversion region at a near zero threshold voltage.

14. (Original) The cell as in claim 11, further comprising:

the transfer gate and a capacitor plate being closer together than a minimum line width of a single photomask.

15. (Original) The cell as in claim 14, further comprising:

a dielectric spacer between the transfer gate and the capacitor plate.

16-29 (Cancelled)